

FIG.1

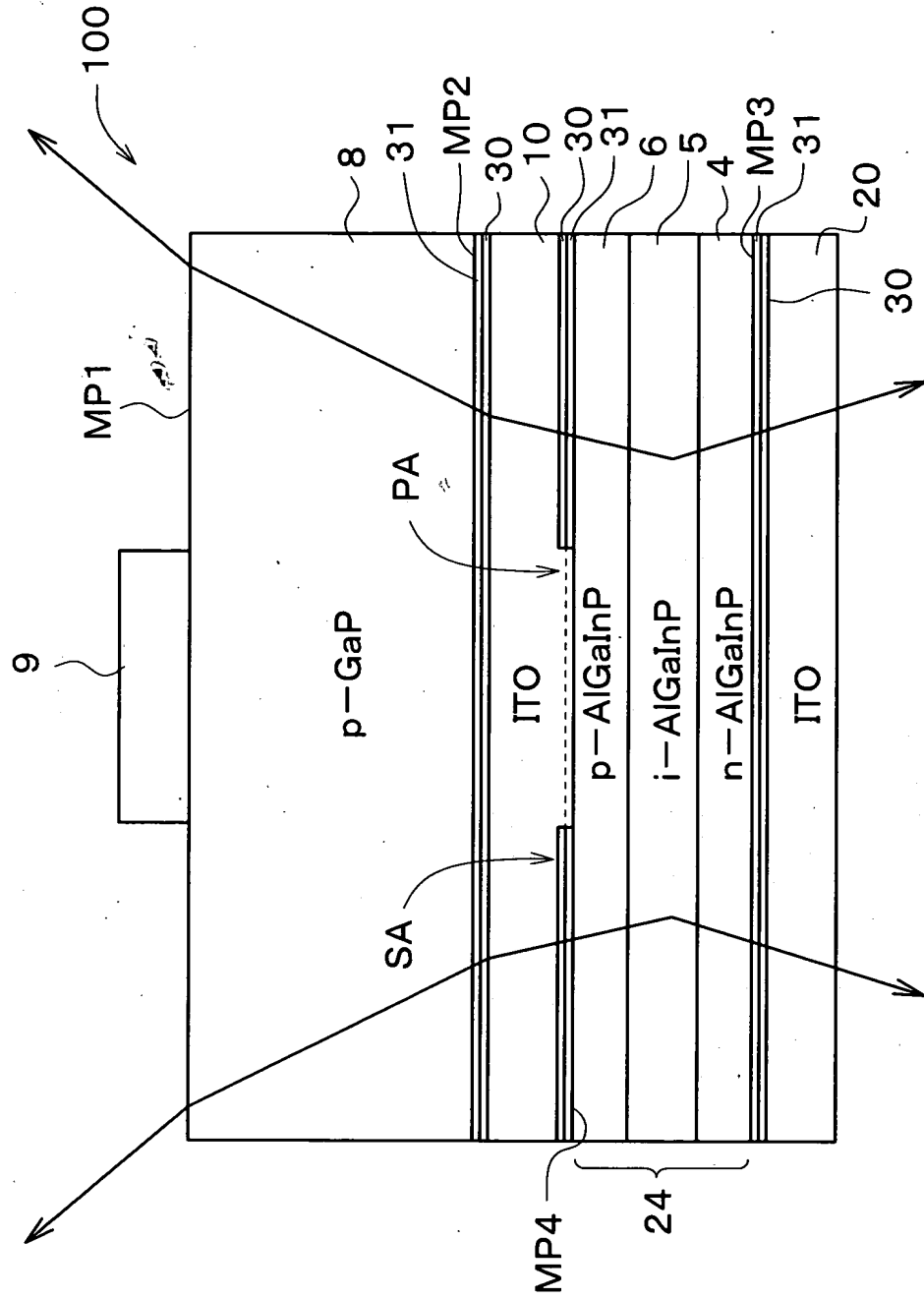


FIG.2

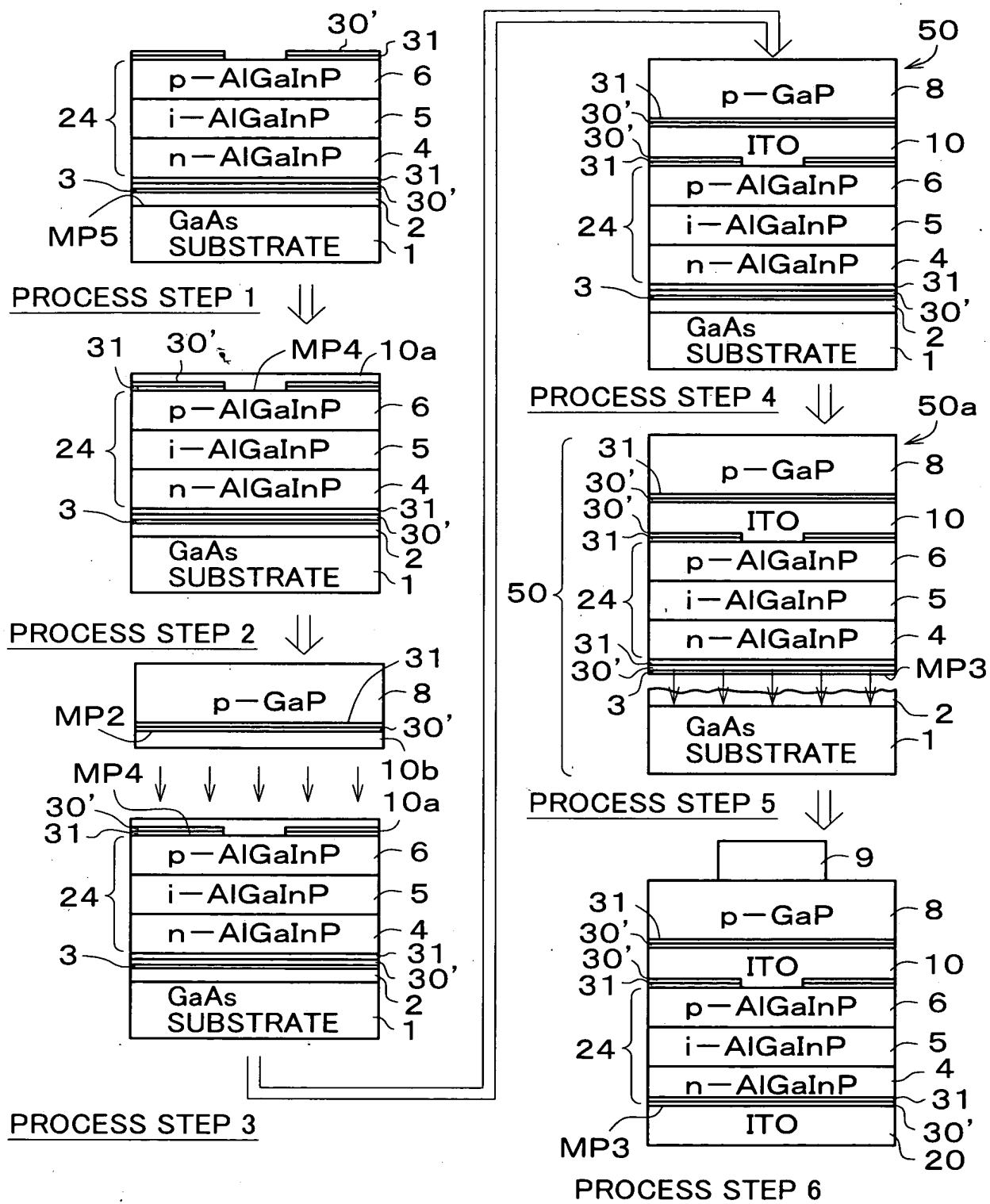


FIG.3

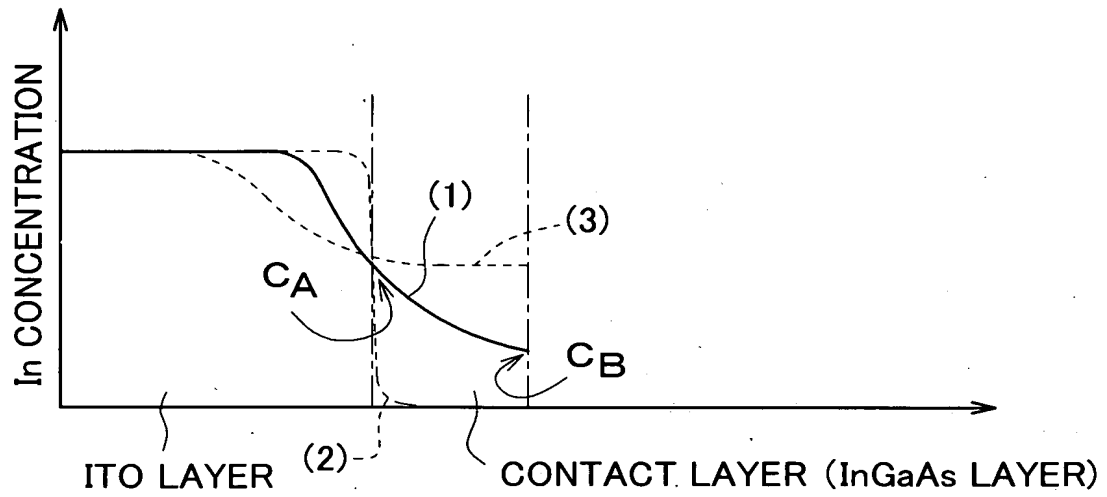


FIG.4

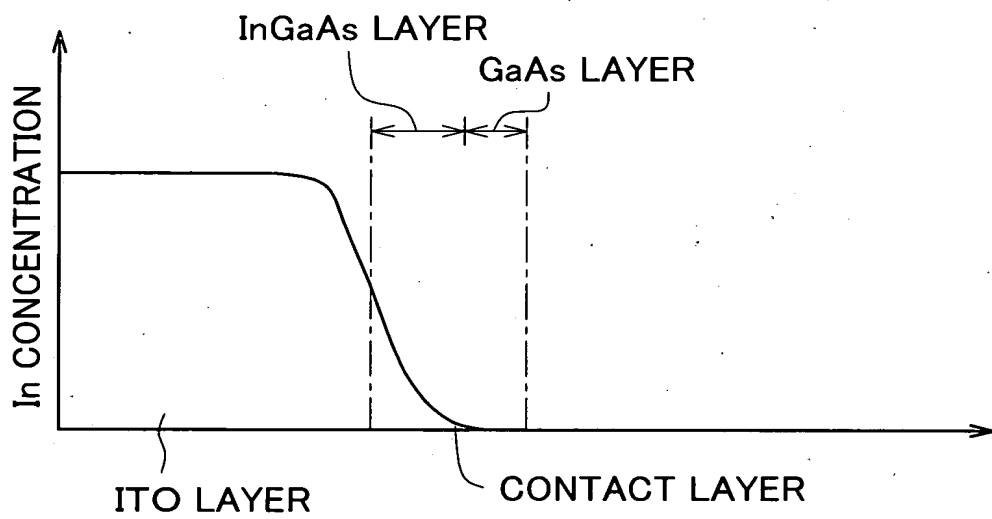


FIG.5

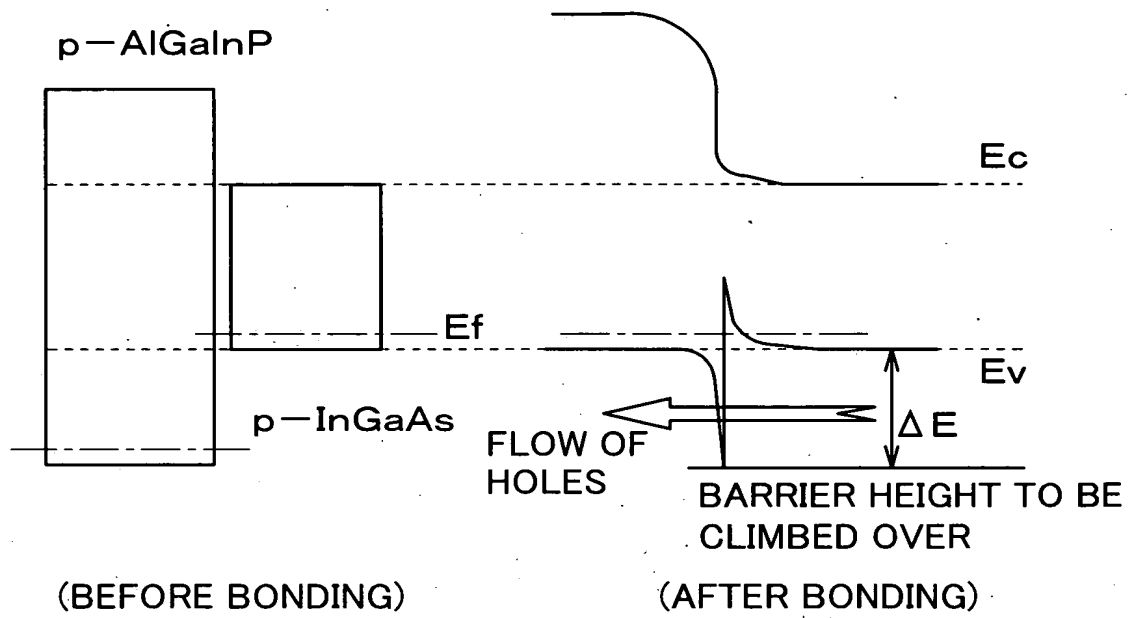


FIG.6

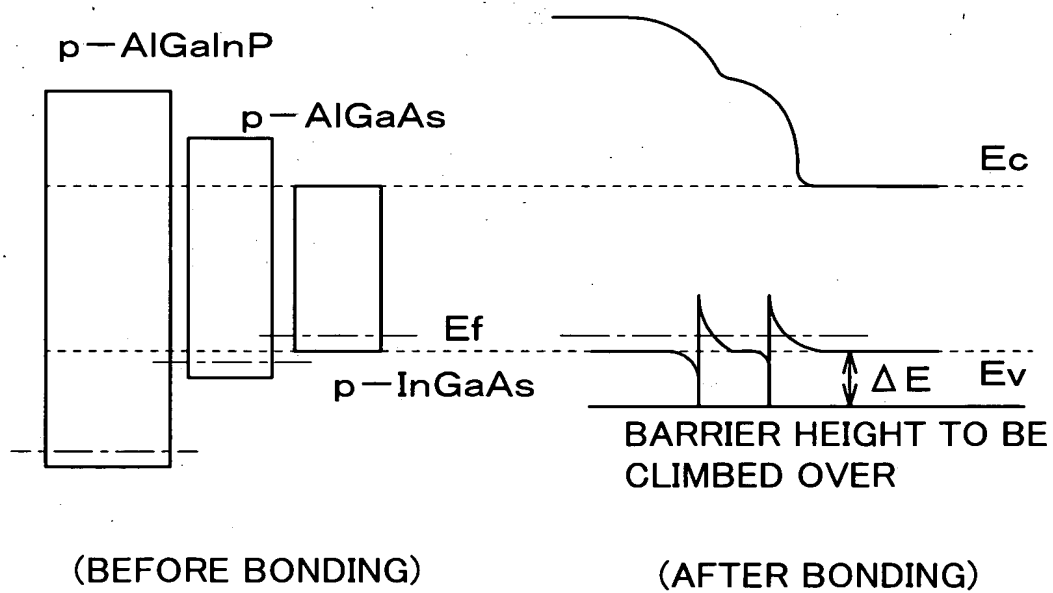


FIG. 7A

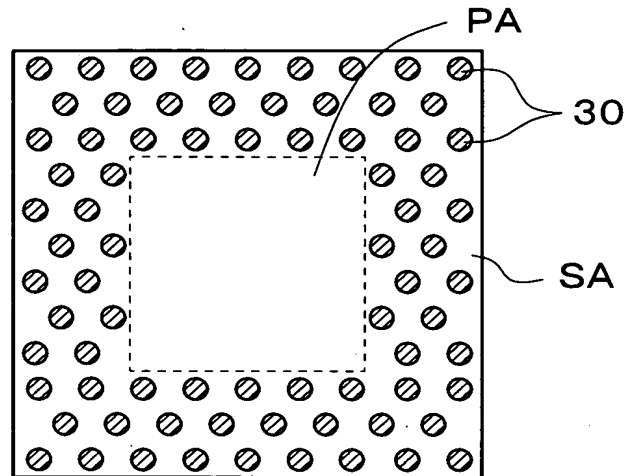


FIG. 7B

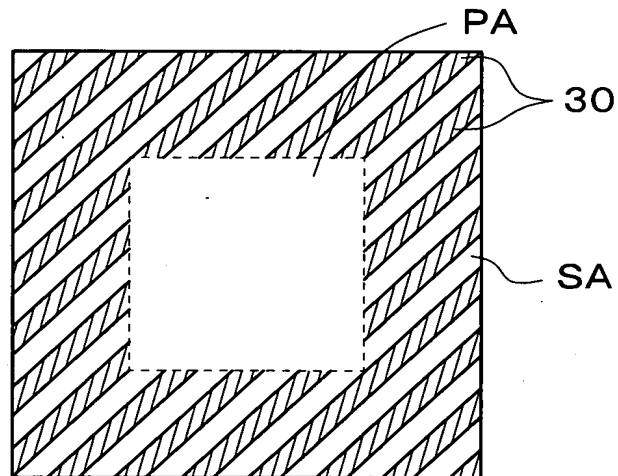
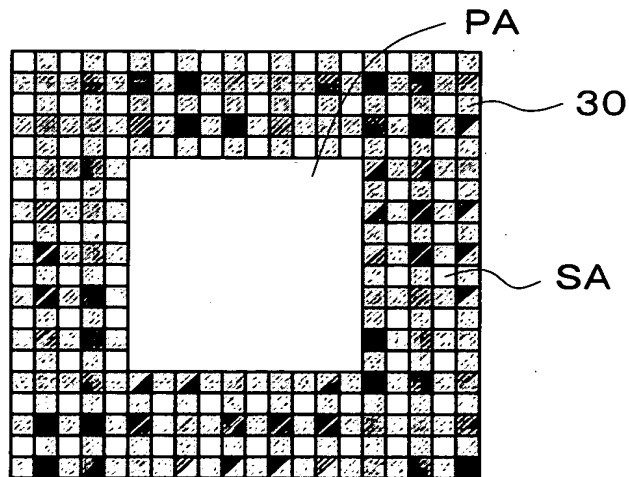


FIG. 7C



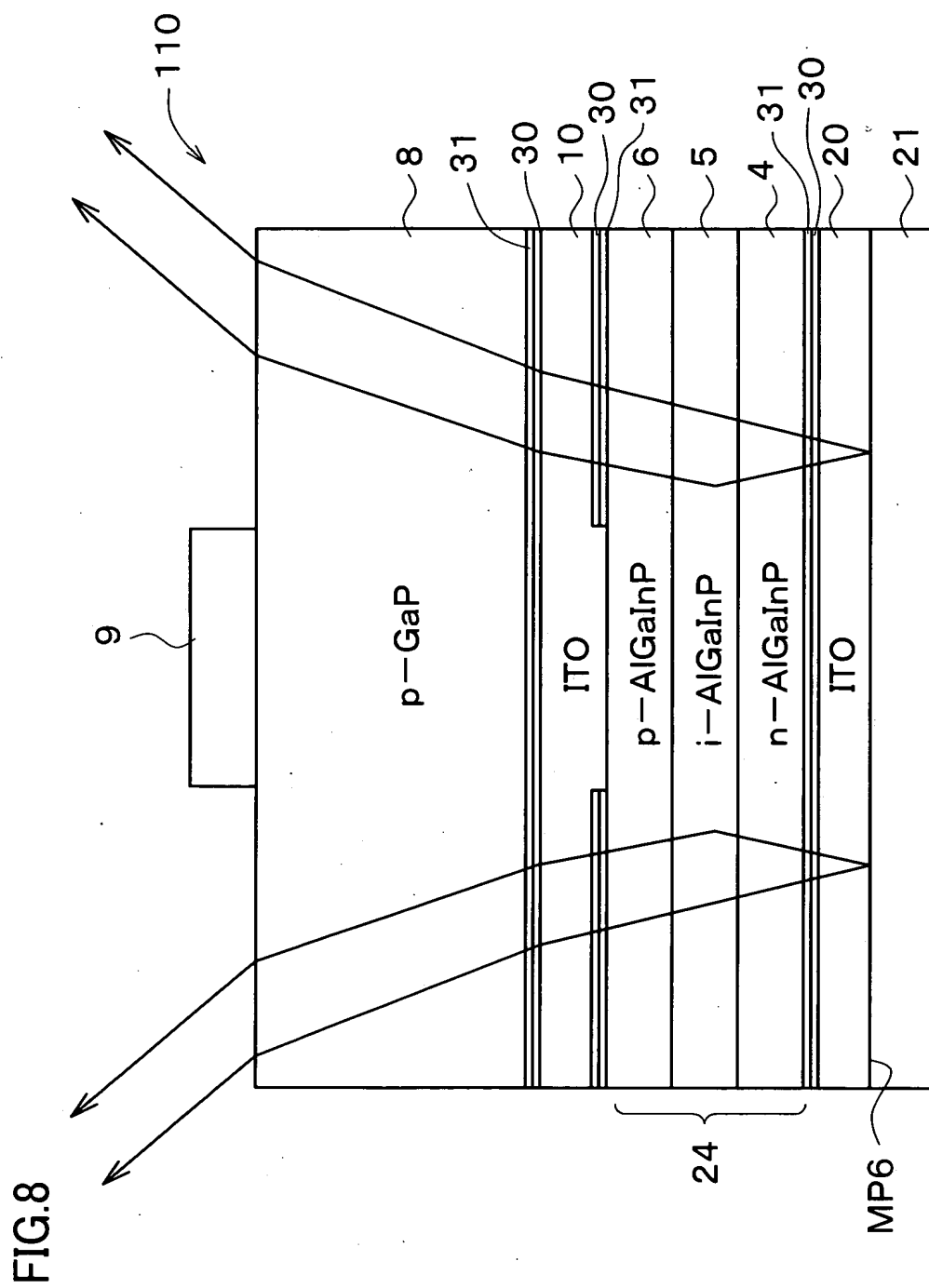


FIG. 9

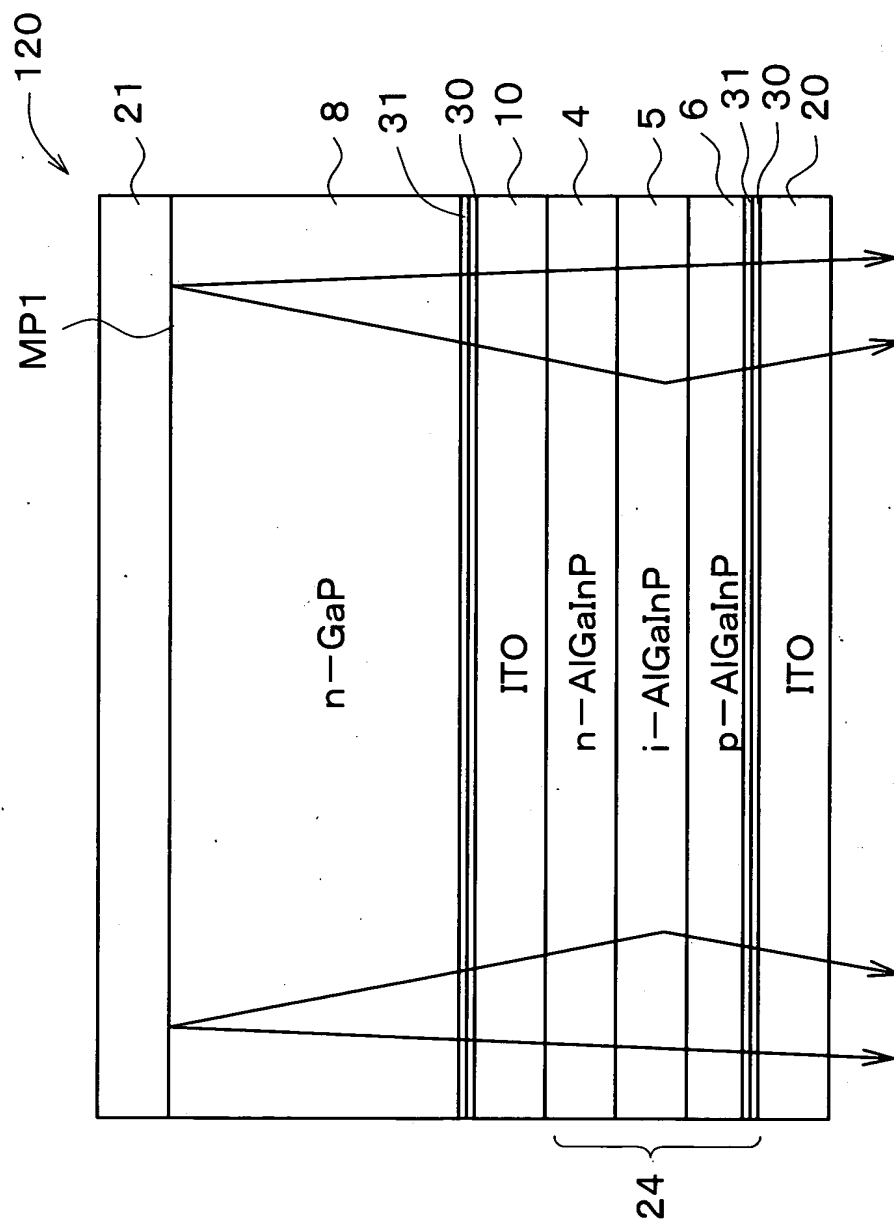
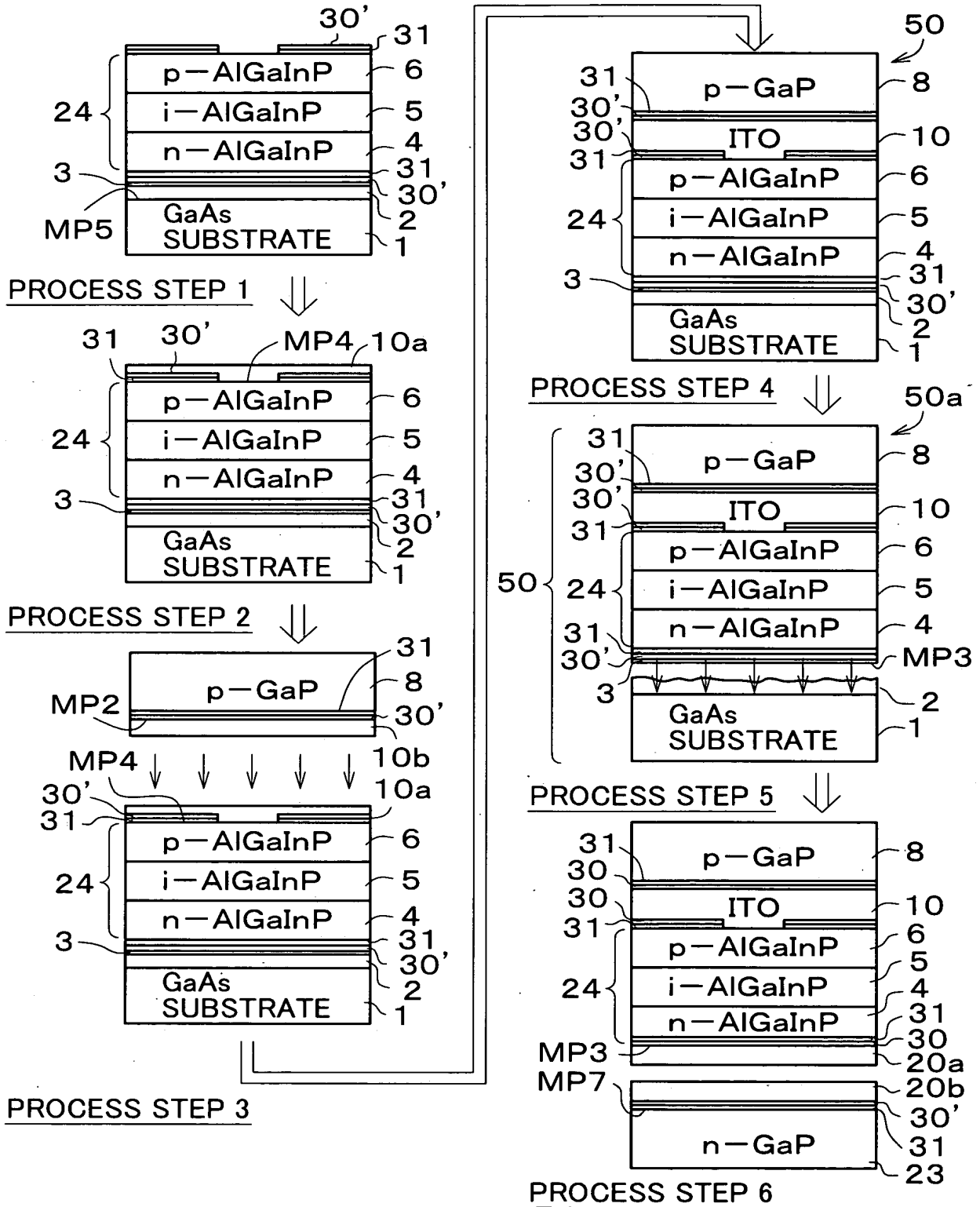


FIG.10



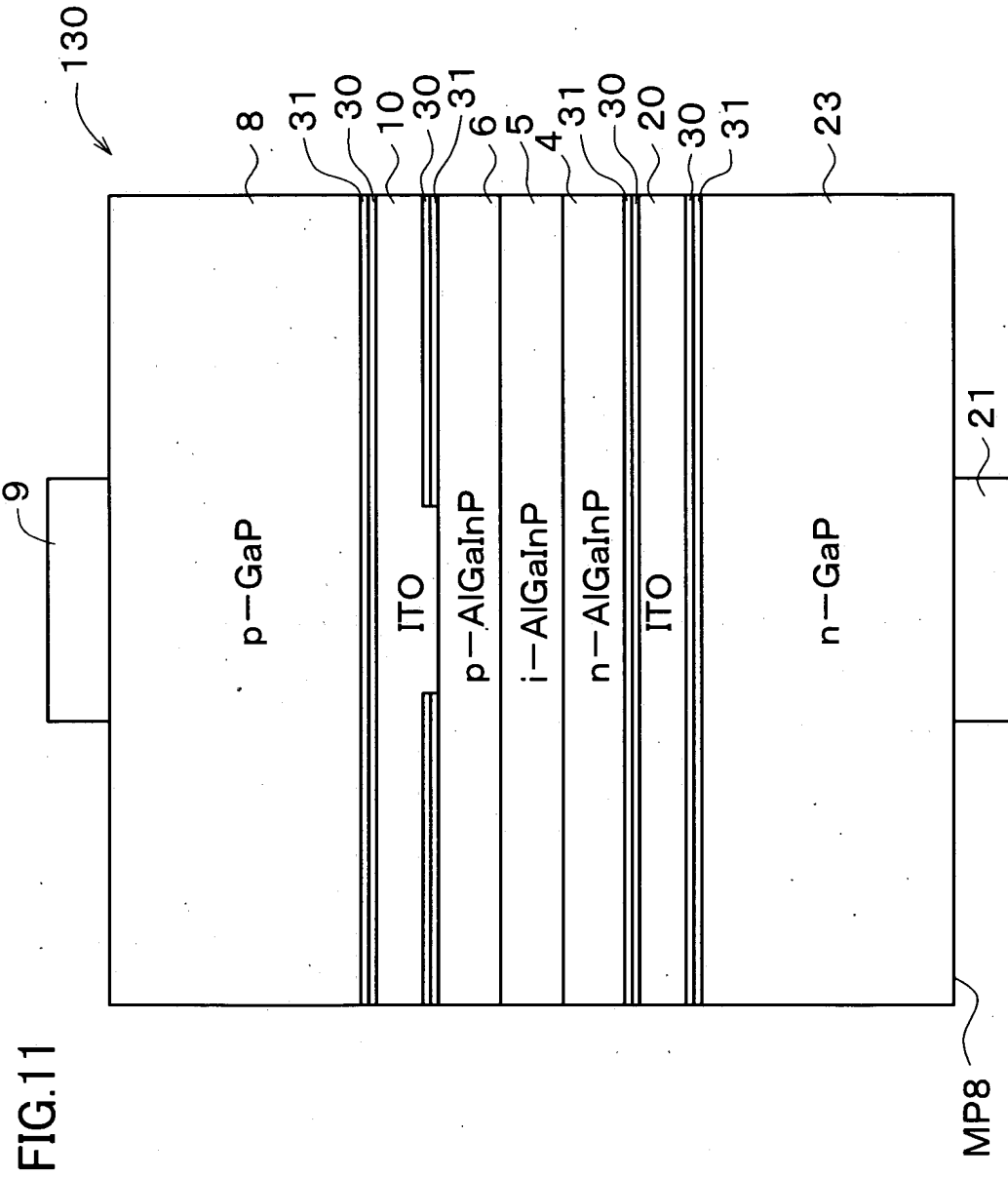


FIG.12

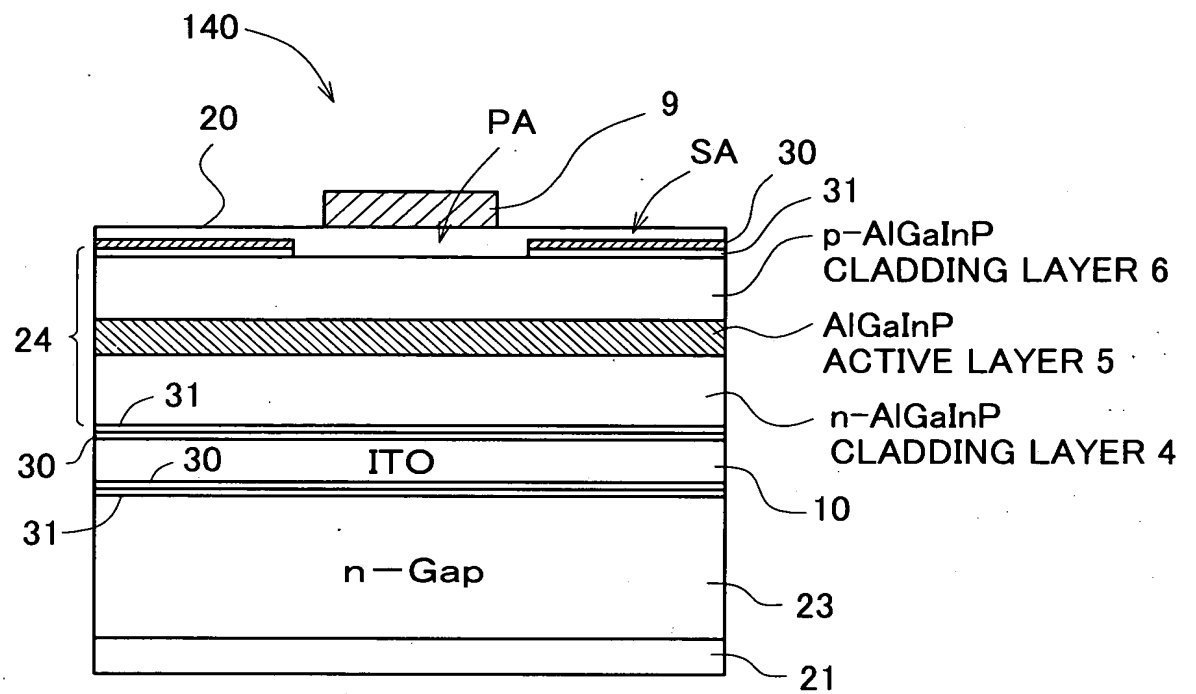


Figure 1 illustrates the fabrication steps of a GaAs-based device, showing cross-sectional views of the structure at different stages:

- PROCESS STEP 1:** Initial structure with layers: n-AlGaInP (4), i-AlGaInP (5), p-AlGaInP (6), and GaAs SUBSTRATE (1). Regions 30' and 31 are indicated.
- PROCESS STEP 2:** Addition of n-GaP (23) layer on top of the p-AlGaInP layer. Regions 30' and 31 are indicated.
- PROCESS STEP 3:** Addition of ITO (10) layer on top of the n-GaP layer. Regions 30' and 31 are indicated.
- PROCESS STEP 4:** Addition of SA (30') and PA (31) layers on top of the ITO layer. Regions 30' and 31 are indicated.
- PROCESS STEP 5:** Addition of n-AlGaInP (4) layer on top of the PA layer. Regions 30' and 31 are indicated.
- PROCESS STEP 6:** Addition of n-GaP (23) layer on top of the n-AlGaInP layer. Regions 30' and 31 are indicated.

FIG. 14

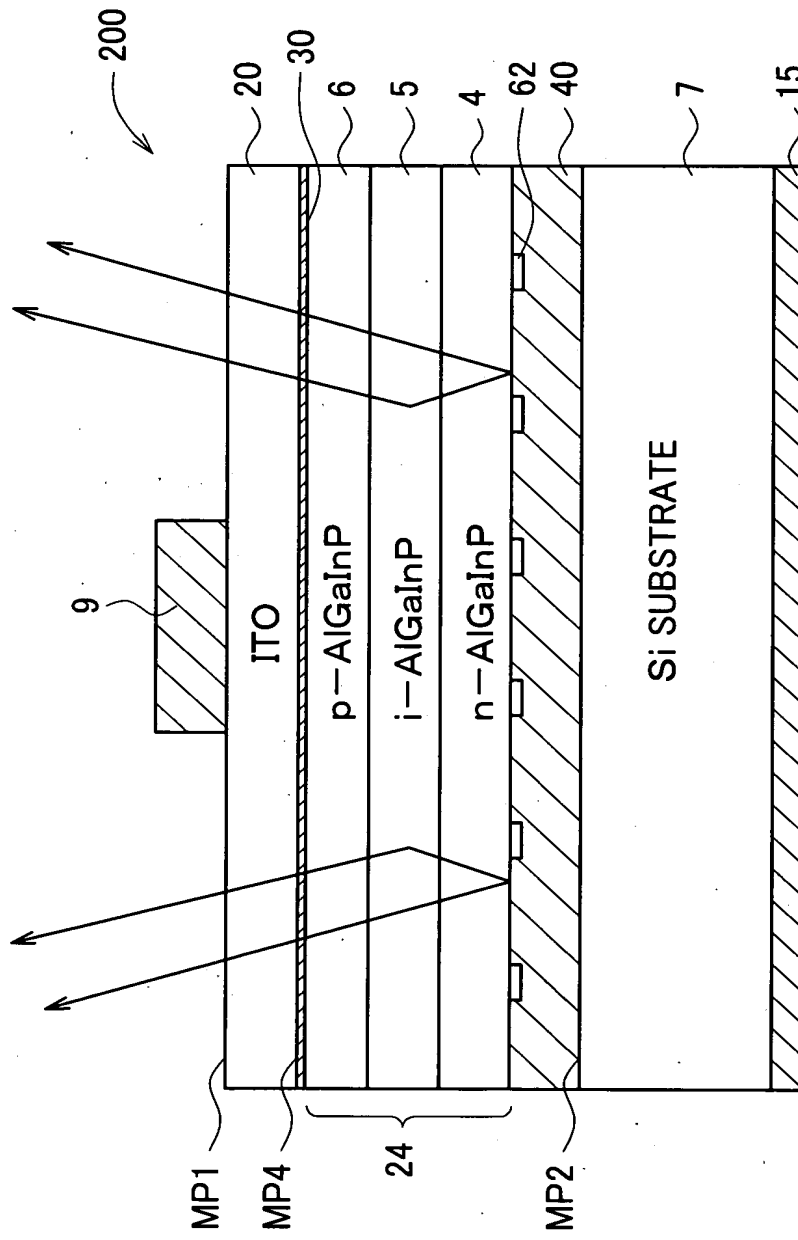


FIG.15

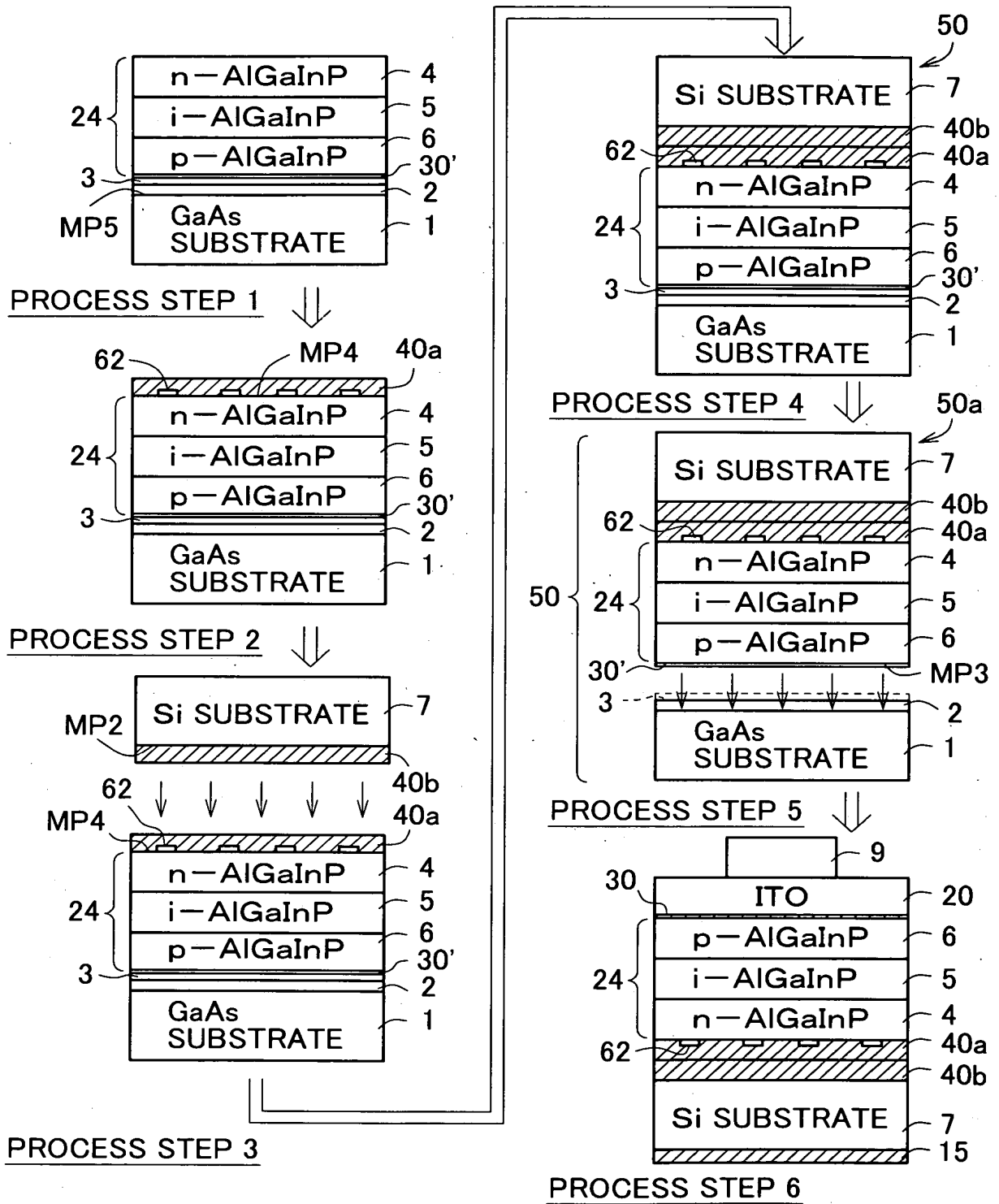


FIG.16

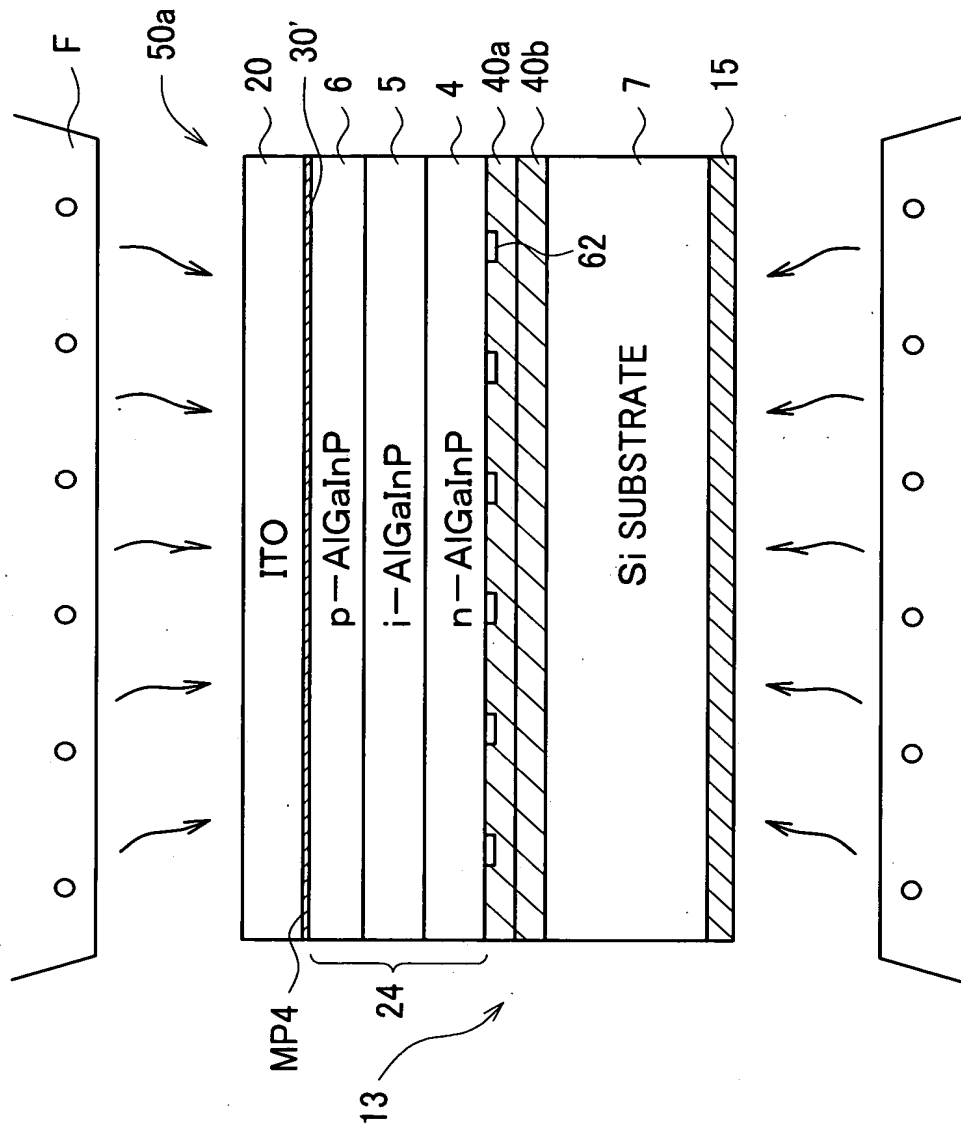


FIG.17

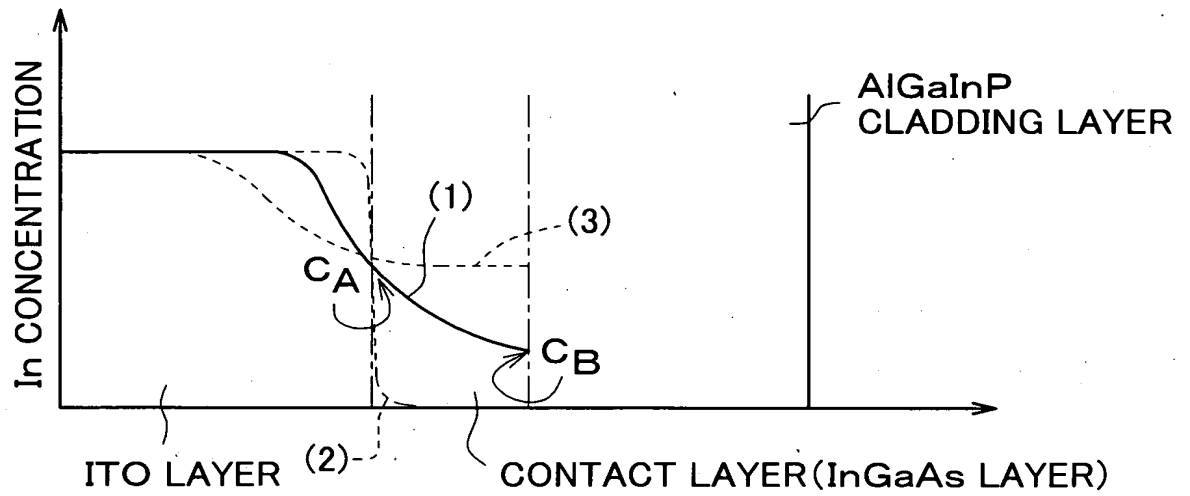


FIG.18

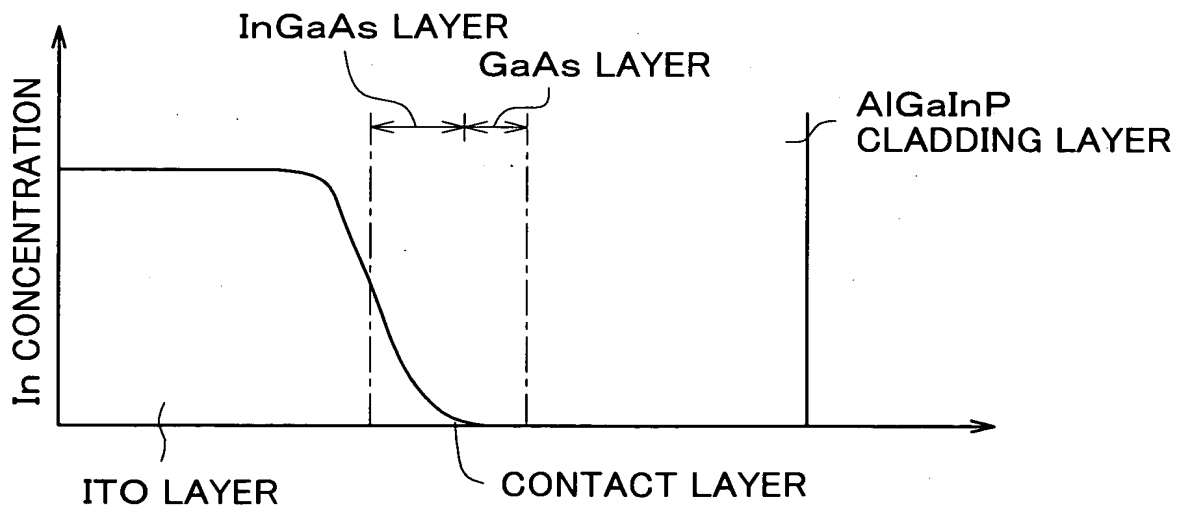


FIG.19

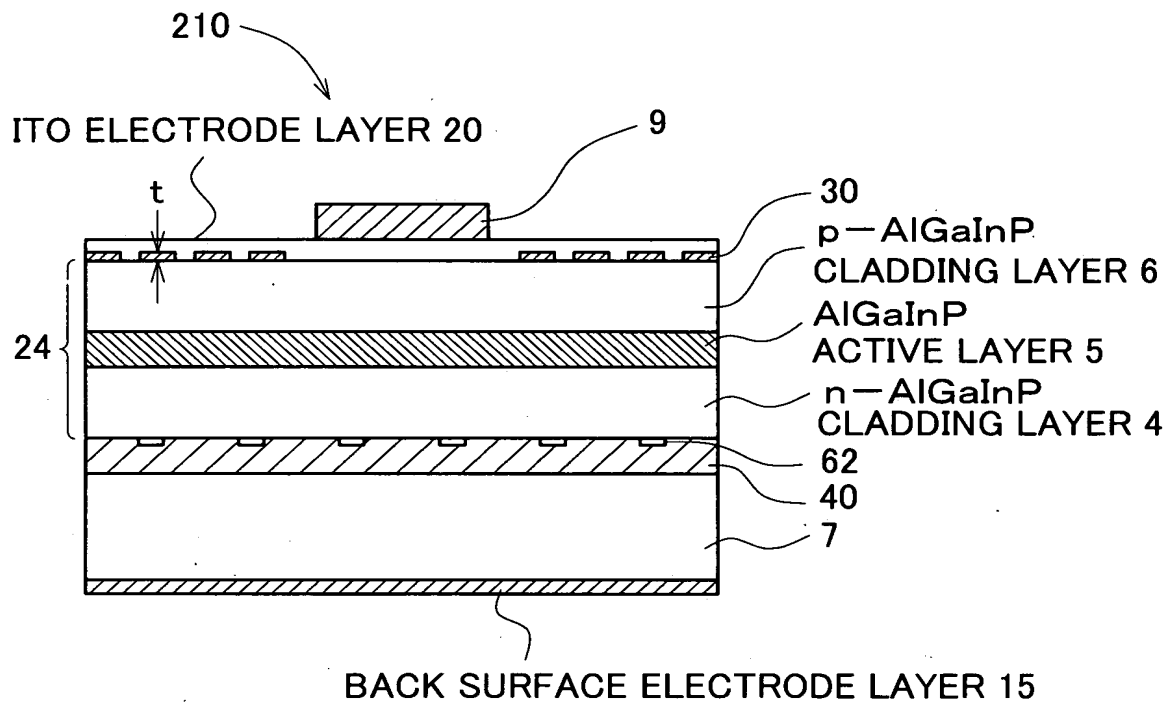


FIG.20

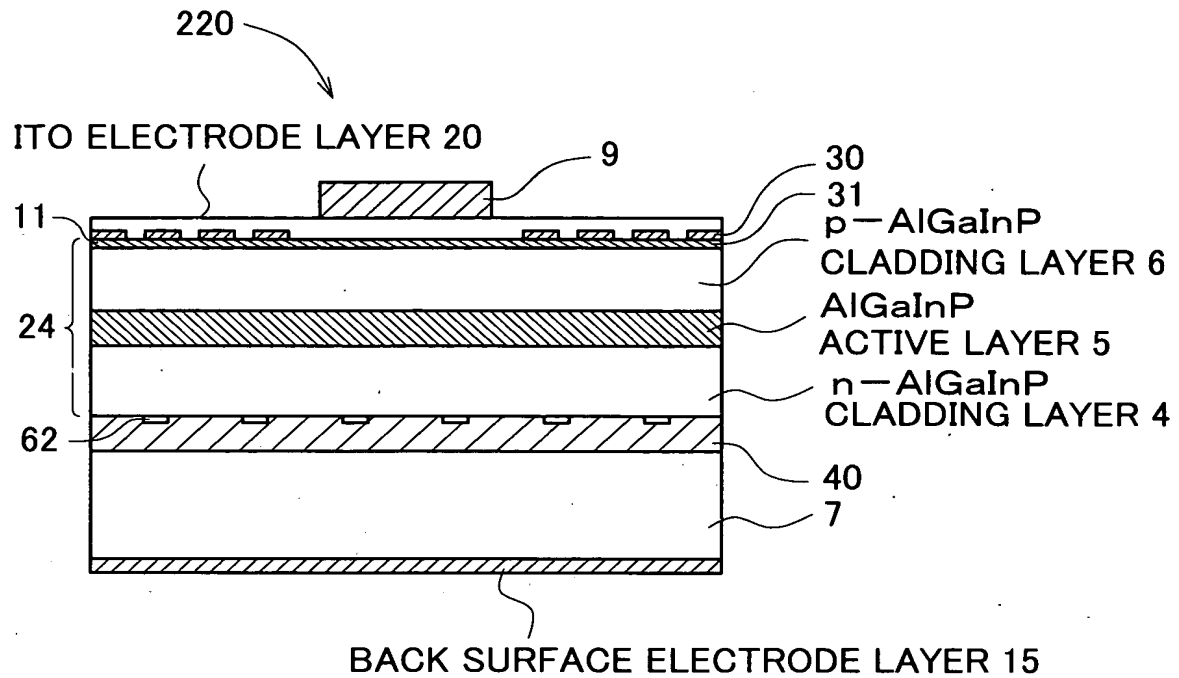


FIG.21

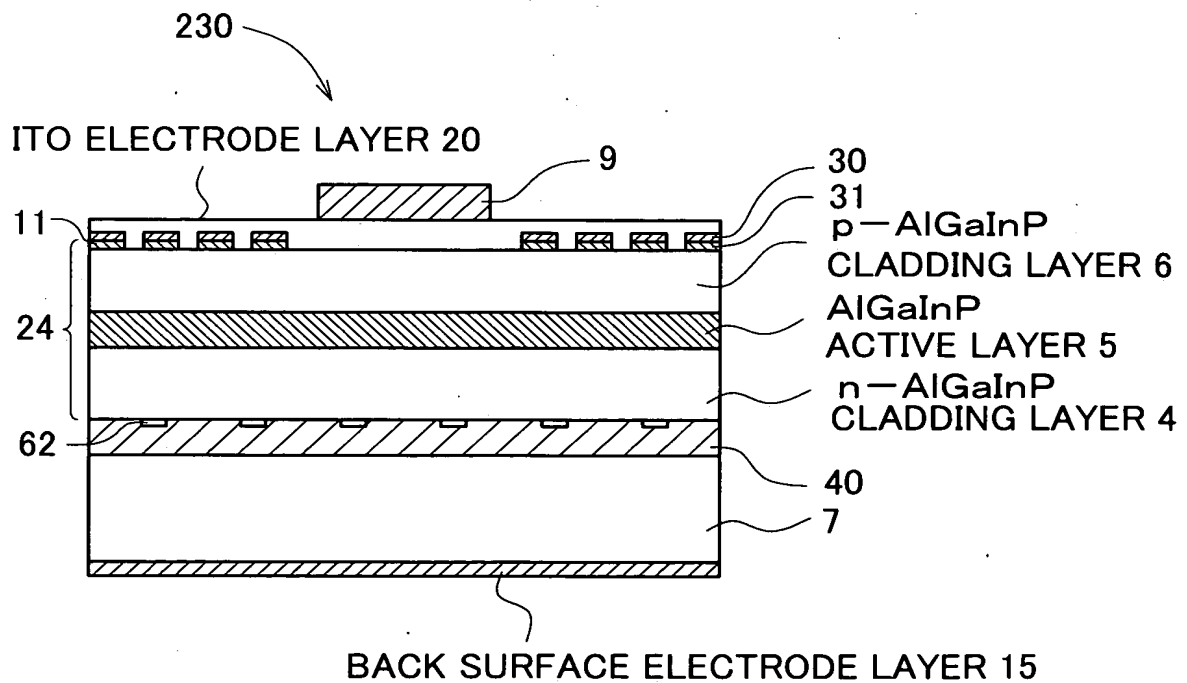


FIG.22

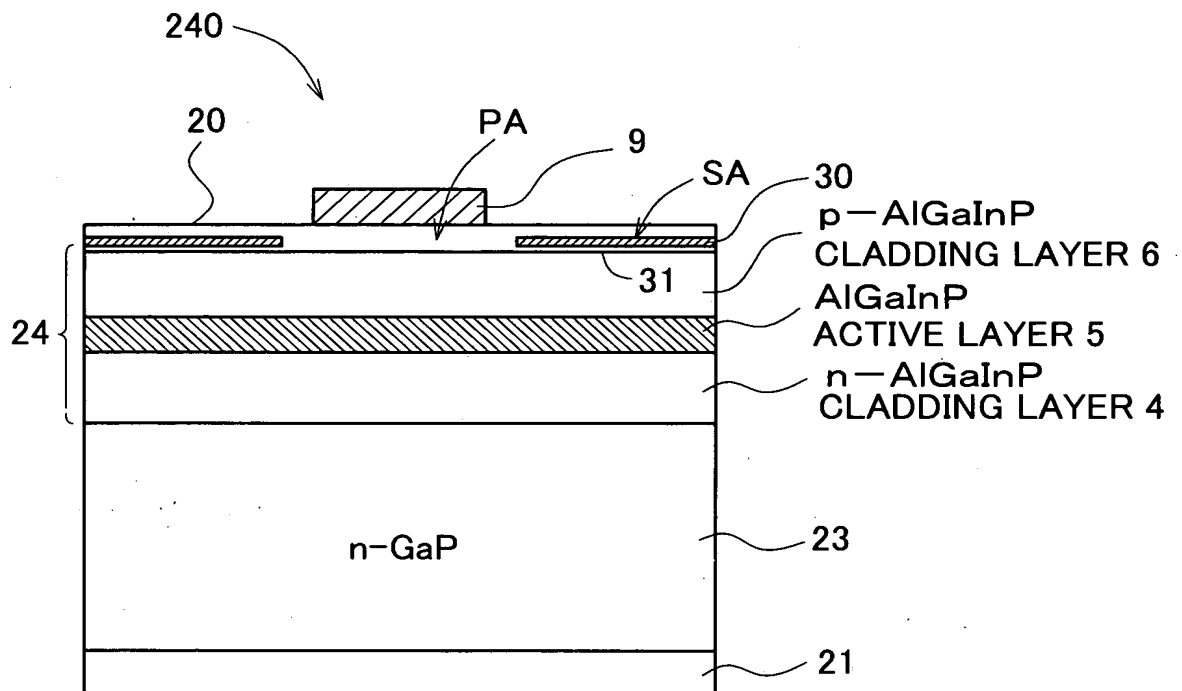


FIG.23

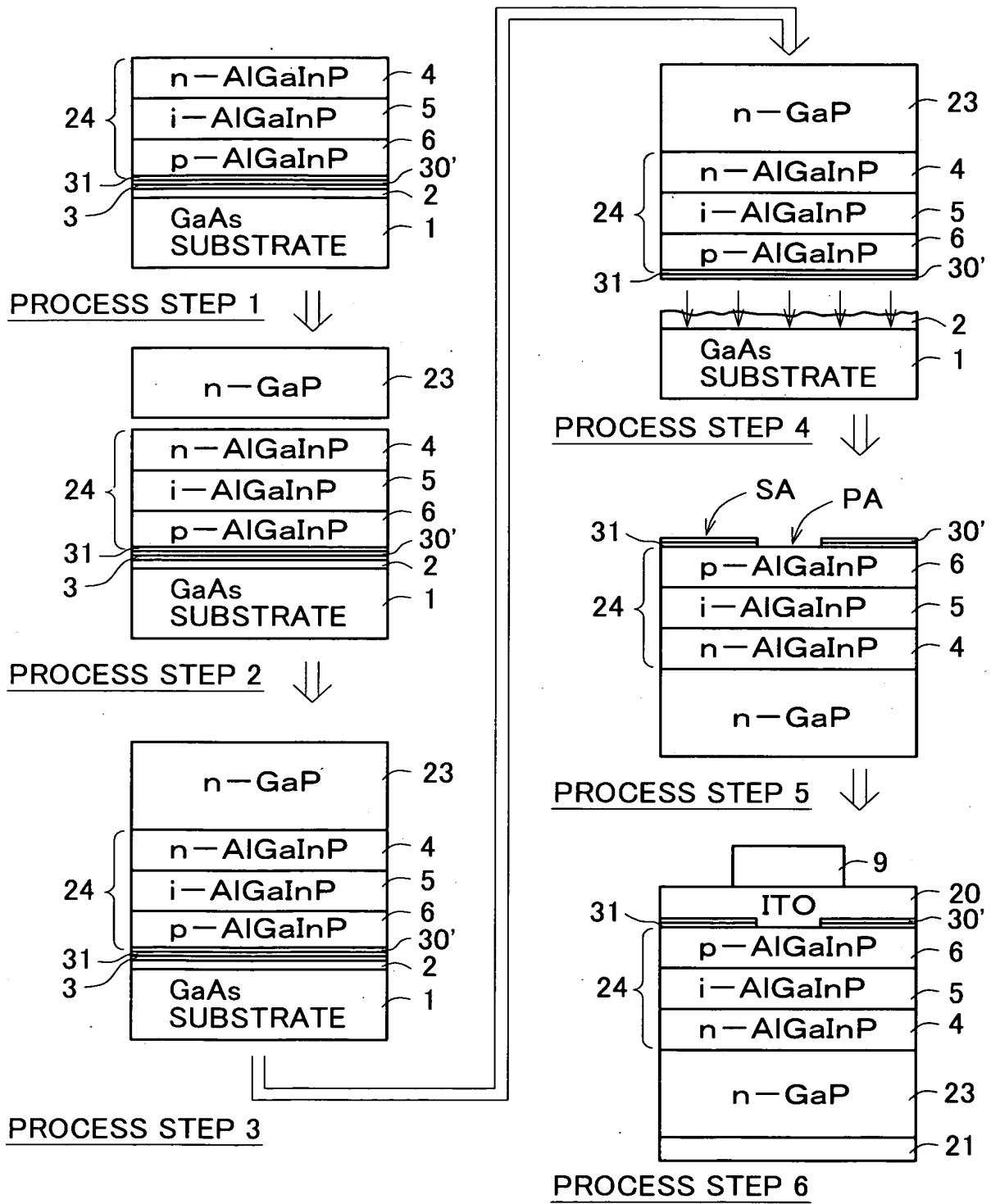


FIG.24

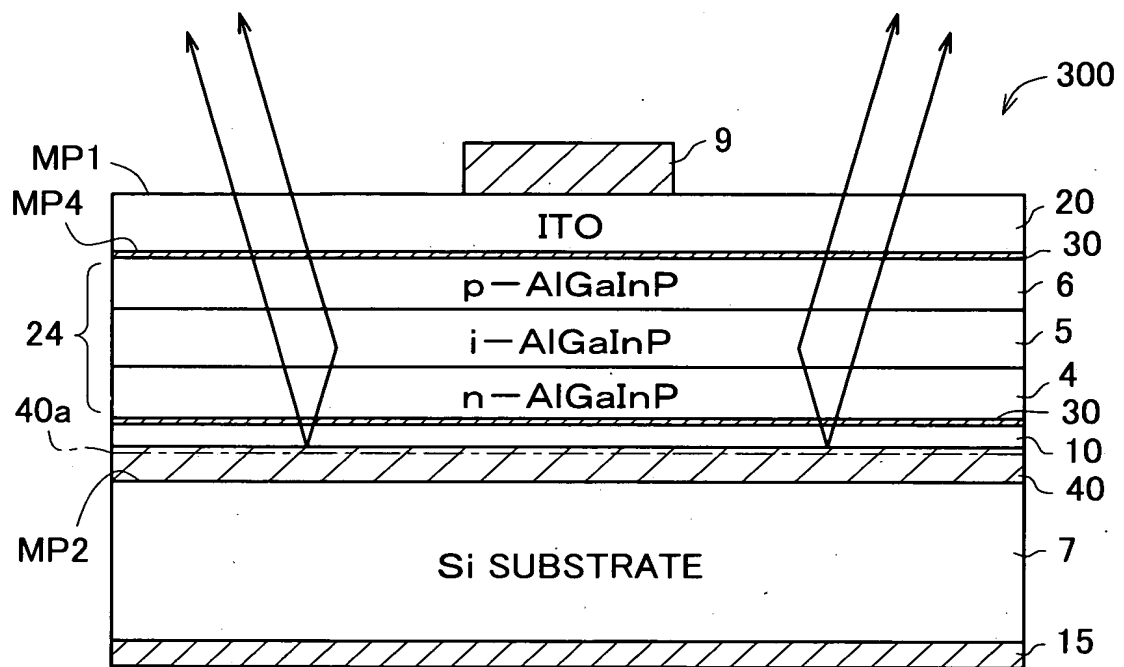


FIG.25

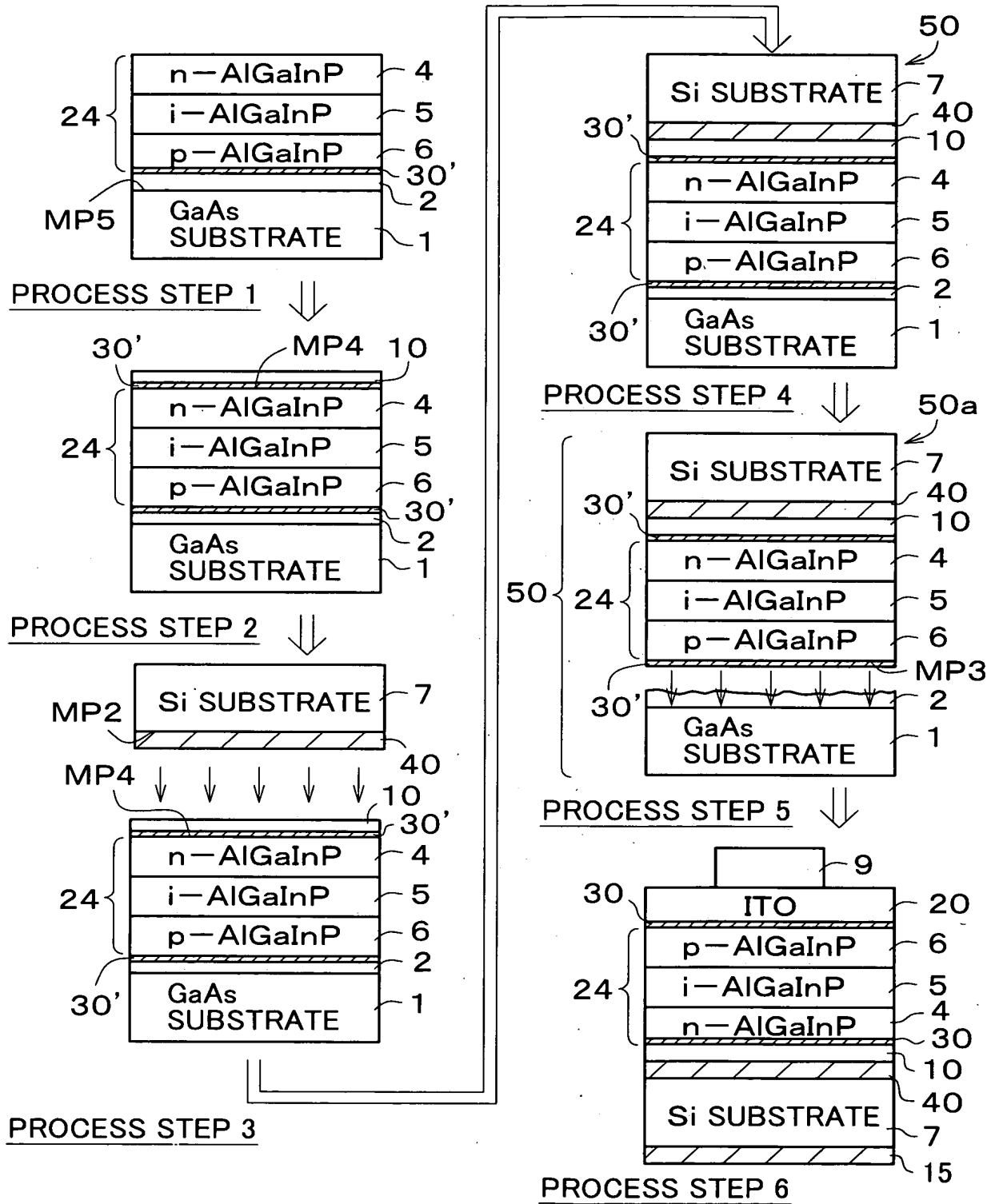


FIG.26

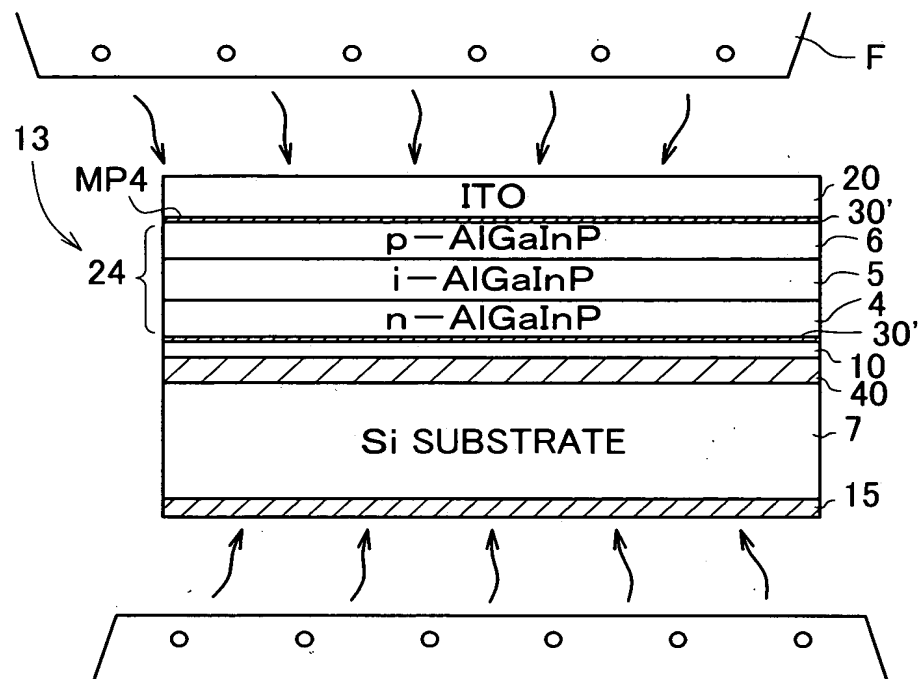


FIG.27

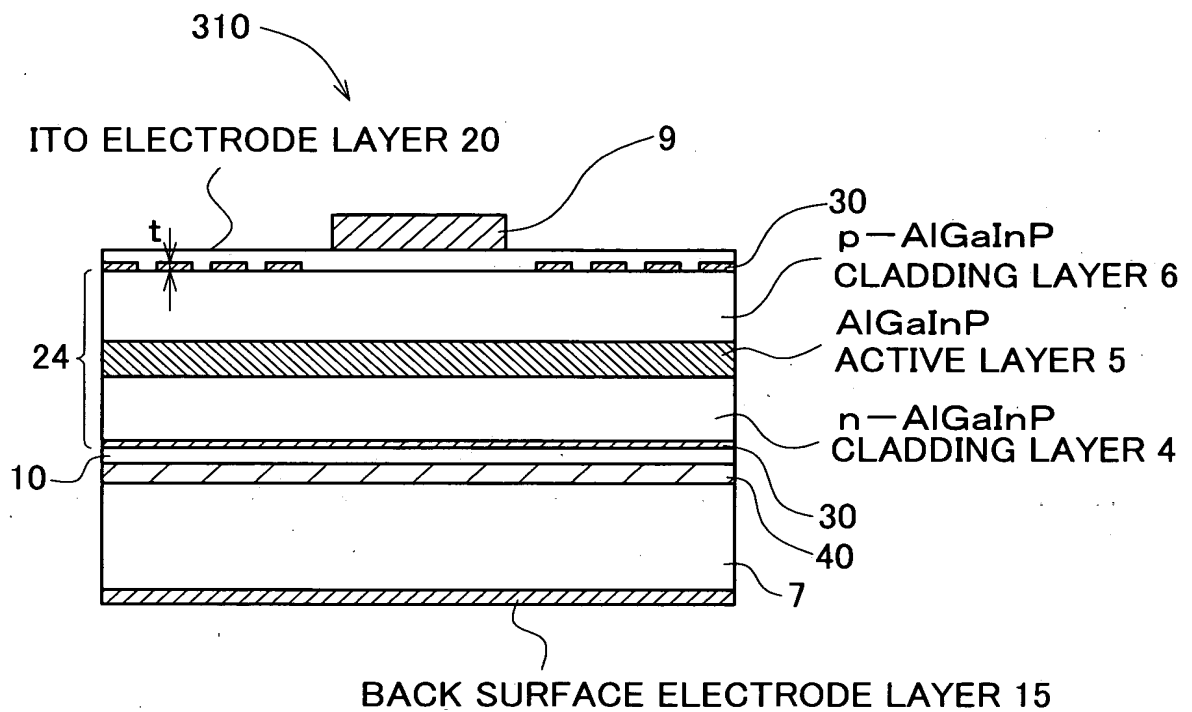


FIG.28

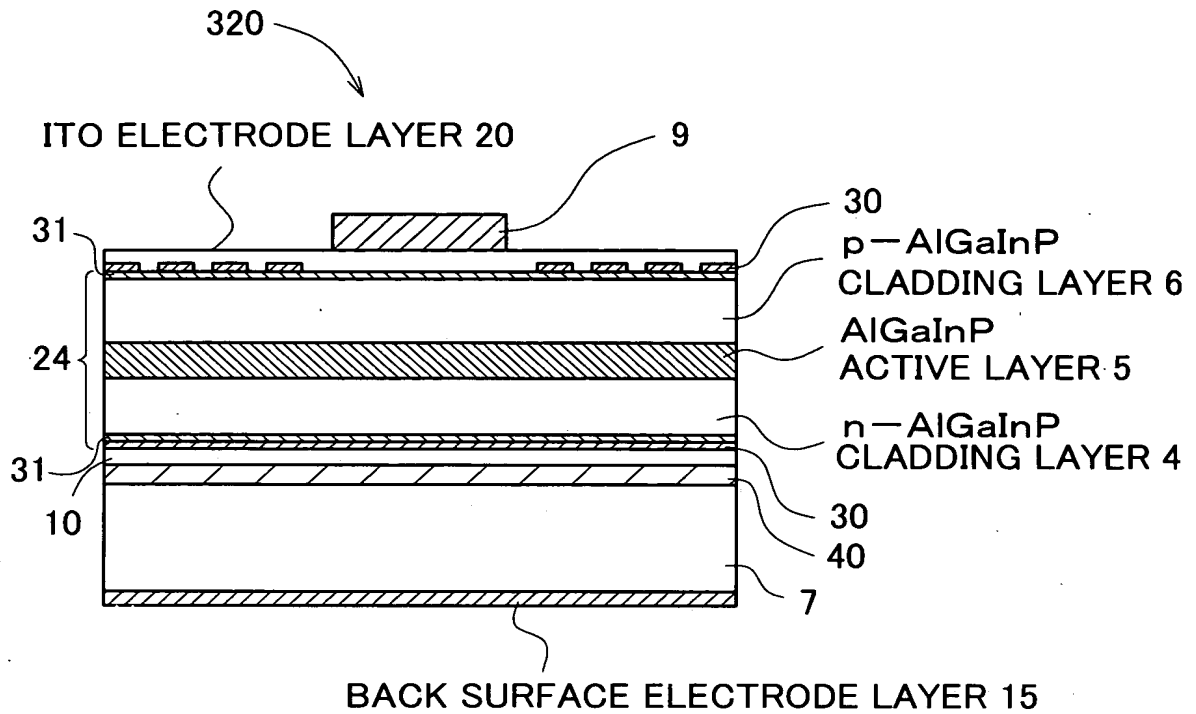


FIG.29

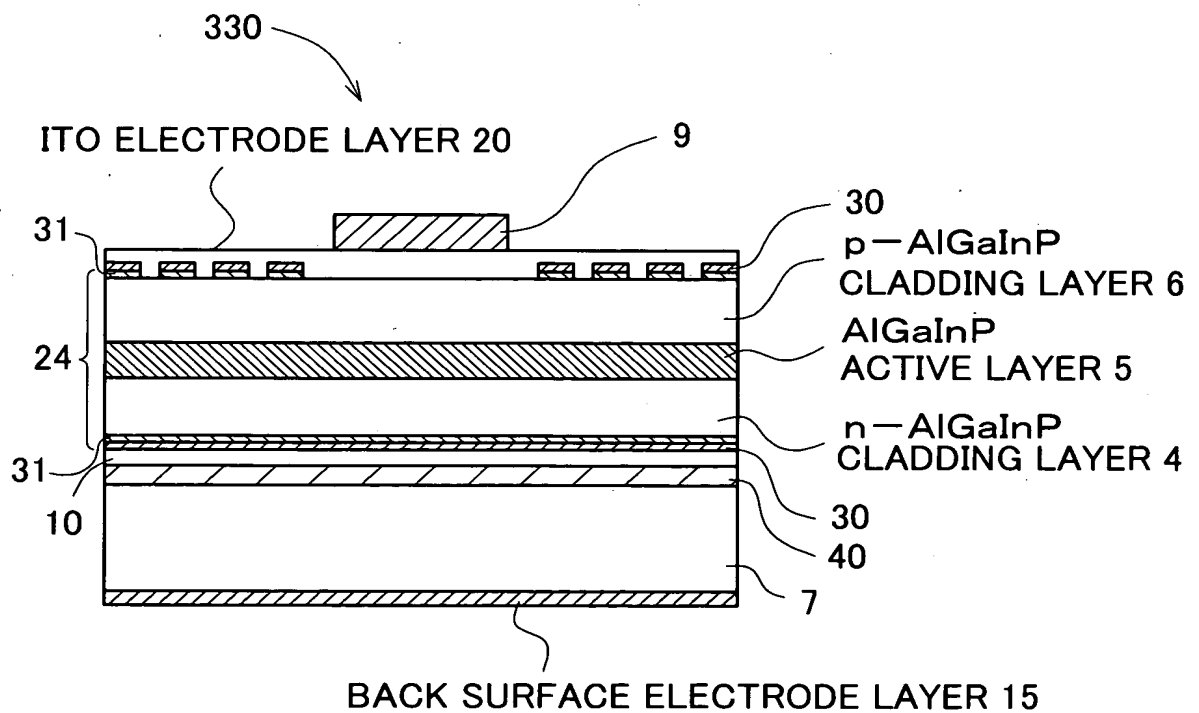


FIG.30

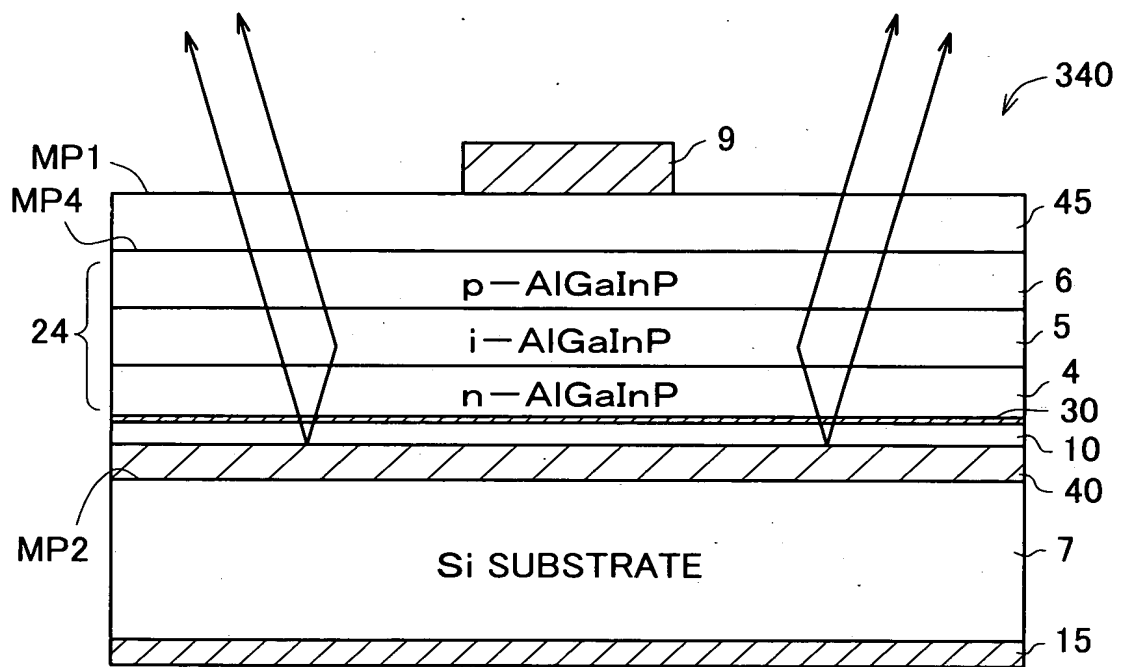


FIG.31

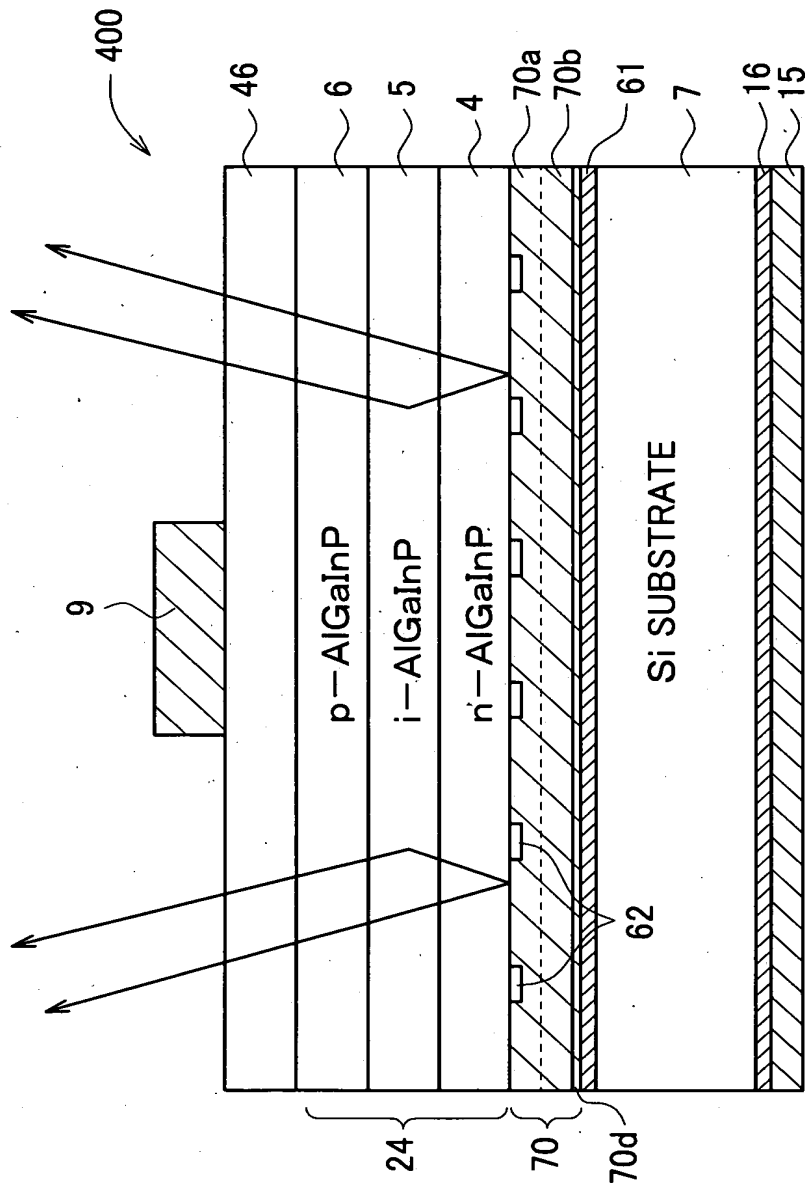


FIG.32

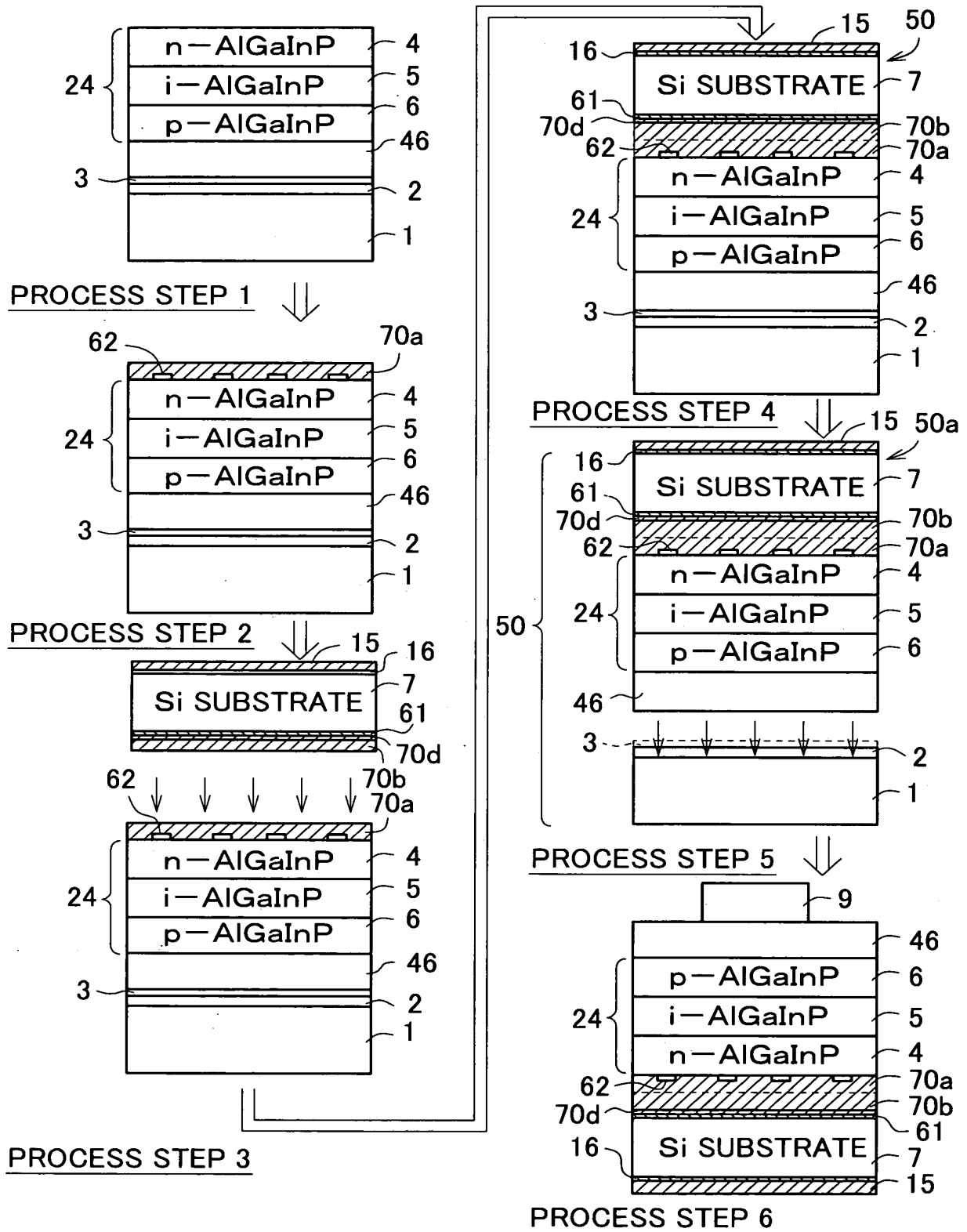


FIG. 33

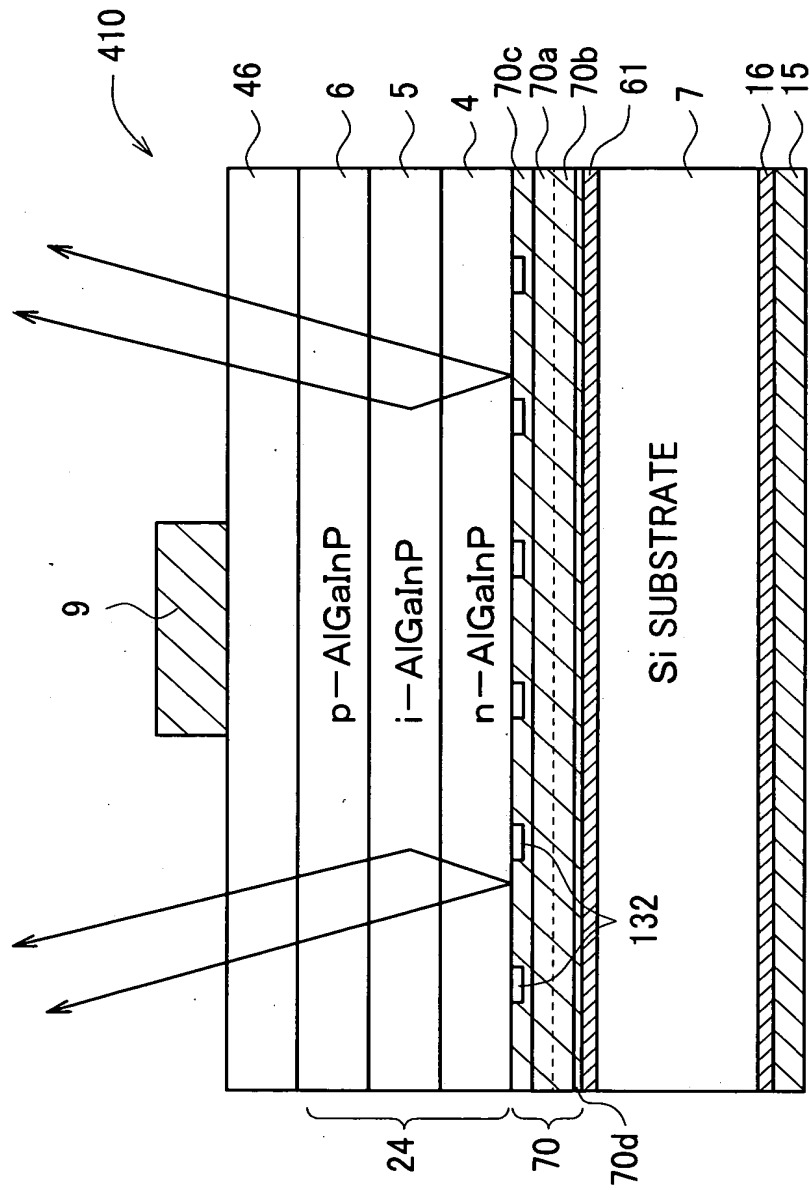


FIG.34

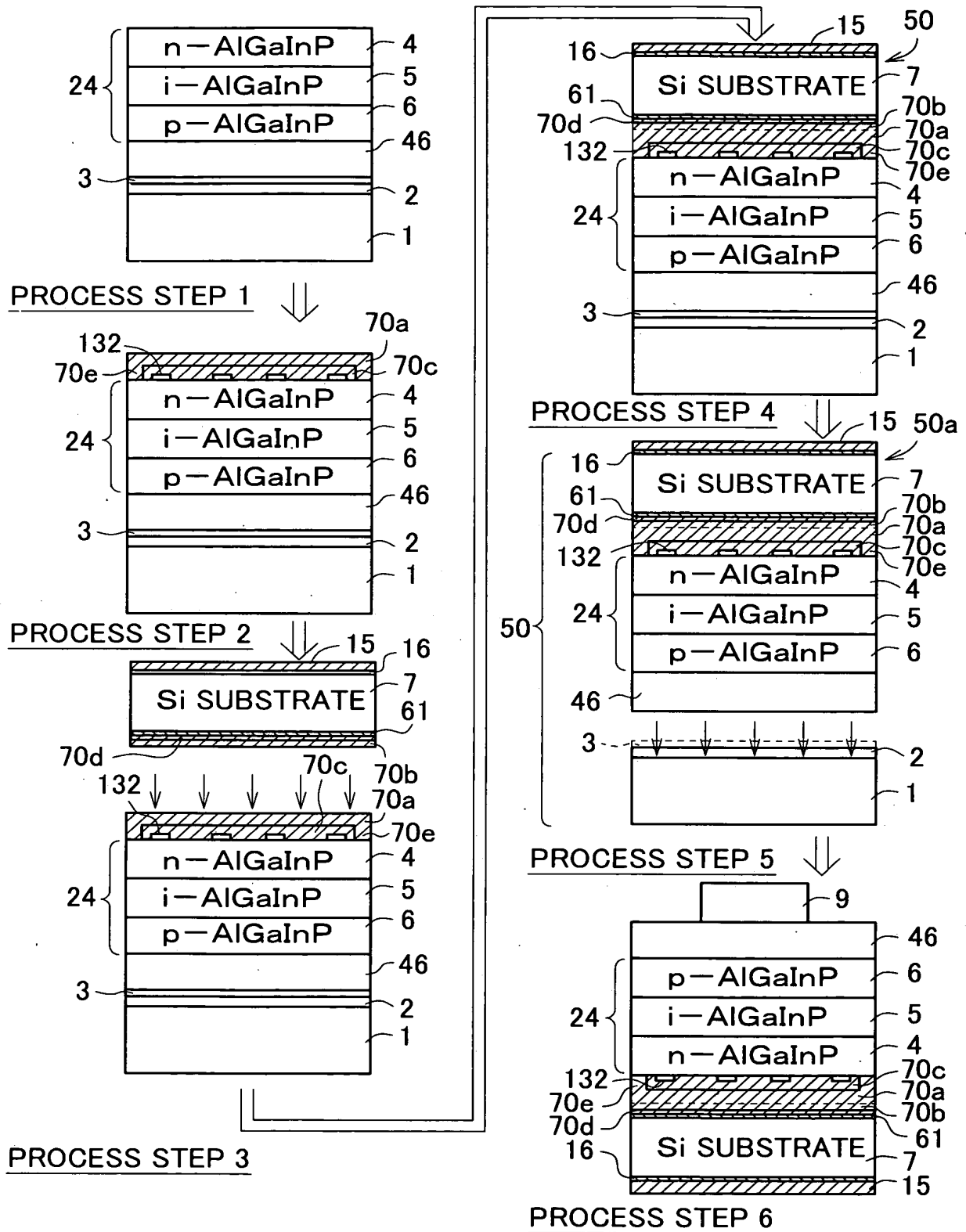


FIG.35

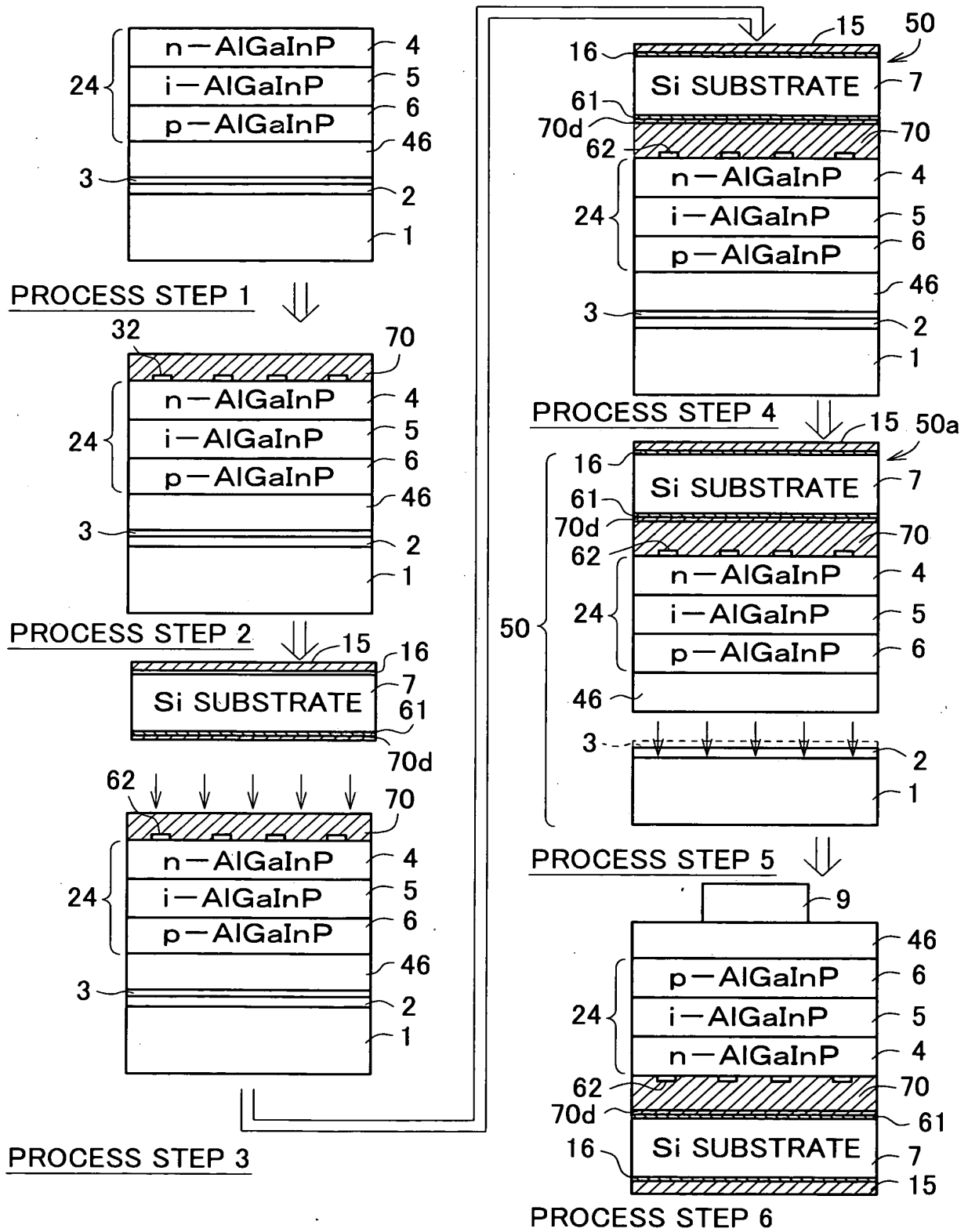


FIG.36

